OLH0608V.A1-940-B

BIDOS® Core

Application

— Proximity Sensing

Features:

— Chip Technology: GaAs VCSEL
— IR Laser Wavelength: 940nm
— Optical Power Class: 10 mW
— Radiation Profile: 21°

Ordering Information

Type	Operational Mode: I_F = 15 mA, T_a = 25°C DC = 100%	Ordering Code
OLH0608V.A1-940-B	10 mW	Q65113A7675

Note: OLH0608V.A1-940-B is a Vixar legacy qualified product.

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1. OPERATING CONDITIONS

Chip is for a Proximity sensing module to be used in mobile phone applications

- Operating Mode: Pulse Mode
- Pulse Width: 1ms
- Duty Cycle: 2.4%
- Typical Operating temperature= 25°C
- Typical Operating current= 15mA

2. WAFER PROBE TEST CONDITIONS

- Operating Mode: CW, DC mode
- Test temperature= 25°C
- Test current= 15mA

3. DEVICE PARAMETER SPECIFICATIONS

3.1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Notes
VCSEL Storage temperature, Ambient		-40 to 100 °C	
Operating temperature, Ambient (VCSEL)	Tv	-20 to 85 °C	
Junction temperature increase of VCSEL		+16°C	Applicable at 15mA, 10.5mW, 1.9V, DC mode, Note 2
Lead solder temperature		260 °C, 10 sec	
CW current (VCSEL)		20mA	(Note 1) in Air
CW current (VCSEL)		25mA	(Note 1) in Other medium (ex: encapsulant)
Laser reverse voltage		5 V	Note 3

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated for extended periods of time may adversely affect device reliability.
Note 2: Temperature is based on when L-I curve begins to roll-over and light output no longer increases with increasing current input. Junction temperature is a combination of ambient temperature and the current through the VCSEL chip.
Note 3: For details refer to the Vixar Application Note "VCSEL EOS/ESD Considerations and Lifetime optimization".

3.2. ELECTRO-OPTICAL SPECIFICATIONS

3.2.1. ELECTRO-OPTICAL CHARACTERISTICS

VCSEL Temp (Tv) = 25 °C, Test current: 15mA. Test condition: CW-DC mode unless otherwise noted.

Parameter	Symbol	Units	Min	Typ.	Max	Notes	Verification
Threshold current	Ith	mA	--	1.8	3.5[1]	In Air	Sampling Basis
Differential resistance	Rs	Ω	--	40	--		100% Wafer Probe
Operating voltage	Vf	V	1.8	2.0	2.05	In Air	100% Wafer Probe
Operating voltage	Vf	V	1.8	2.0	2.05	In Encapsulant	Sampling Basis
Optical operating power	Lop	mW	10.0	11.5	--	In Air	100% Wafer Probe
Optical operating power	Lop	mW	7	11.5	--	In Encapsulant	Sampling Basis
Slope efficiency	SE	W/A	--	0.95	--	In Air	Sampling Basis
Beam divergence	$1/e^2$	deg	--	21.5	25	In Air	Sampling Basis
Operating wavelength	λop	nm	930	940	950	In Air & Encapsulant	100% Wafer Probe

Note 1: It is observed that there is a difference between 100% wafer test versus die sample testing. At die sampling test, Ith maximum is 2.5mA. This correlates to a maximum 3.5mA at wafer level.

3.3. MECHANICAL ROBUSTNESS SPECIFICATIONS

Stress	Description
Bond pad adhesion	Wire pull reliability > 3g pull force. (Tested on a On-going basis)

3.4. DEVICE RELIABILITY SPECIFICATIONS

Stress	Description
VCSEL reliable lifetime Requirement	5 years of life time at Operating condition.
Intrinsic Failure rate	≤5 FIT at 60%CL, 25°C Tambient
Early Failure rate	≤20ppm

Note 1: Failure criteria is defined as either a drop in optical power of ±30%, Vf ±10%, a gross mechanical failure, or violation of specification.

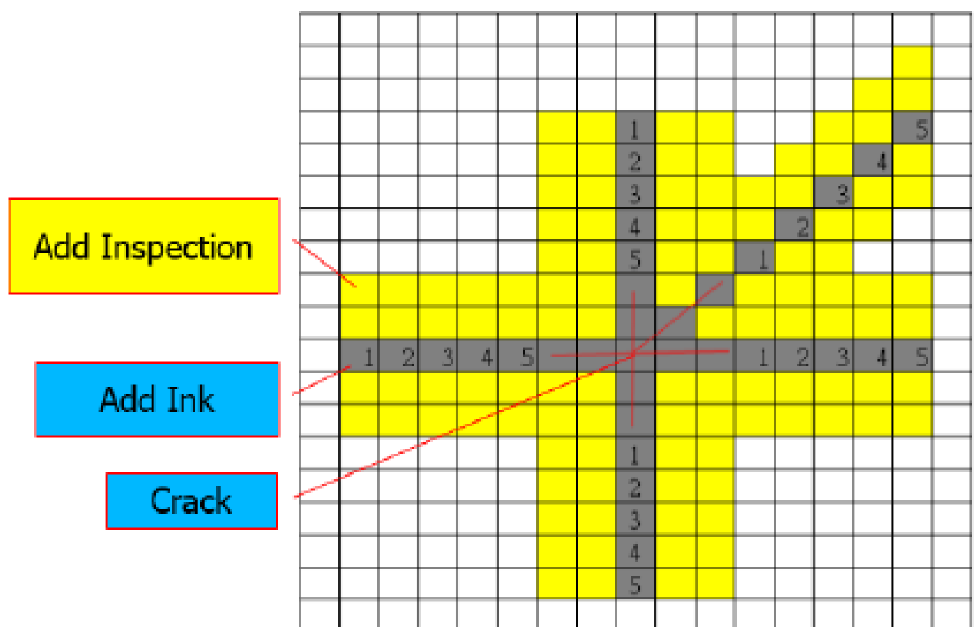
3.5. OPTICAL INSPECTION OF WAFER/DIE

Diced and singulated VCSEL wafers are 100% screened using automated optical inspection tools to ensure adequate cleanliness and that die are generally void of defects, stains, scratches, marring, cracks, and chips. Die are screened to the following metrics:

Variable	Description
Emission area	Defect in emission area > 8 µm
General reject	Defect in die area (except emission area) > 12 µm
Chip out	City moat area > 10 µm
Aligner fail	Die has location issue, AOI can't align
Inked	Die rejected by general inspection (manual)

Wafers that break during the fabrication process are scrapped and removed from production. If a wafer breaks after fully completing wafer fabrication, it can still be used in production if the sections are large. Wafer breakage under this condition is defined as a wafer breaking or cracking after it has been through final backside thinning and before being mounted to dicing tape. Typically, this occurs during handling at wafer probe. Standard broken wafer shipping criteria is that the wafer is OK to use if a wafer has broken into no more than 2 pieces and the

section are larger than approximately 60 mm^2. Inspection protocol for broken wafers is a manual inspection that inspects die found near wafer cracks with the following procedure:



Die are inked following the crack direction (left to right, top to bottom, or oblique line, depending on the direction of the crack), noted as the red line in the image above. Die are inked until there are no more die effected by the crack. An additional 5 die are also inked along the same direction that are past the extent of the visible crack to prevent die that may be affected by micro-cracks. Die surrounding the affected area, defined by the yellow region in the image above, receive additional, more intensive inspection to ensure they are not damaged and are inked if needed.

3.6. WAFER QUALIFICATION

Vixar products, in this case VCSEL die go through a reliability qualification process to determine the fitness of the product to meet customer lifetime requirements. This involves stressed aging of packaged parts sampled from finished wafers under high temperature and operating currents to determine the wafer reliability. Typically, 32 VCSEL die will be selected from across a production wafer and assembled for testing. These qualification parts will be subjected to stressed conditions of 16mA CW current at 105 °C for 168 hours (1 week). The LIV of each die is read out before the test is initiated and after the test is complete. A fail is considered any die that has a decrease in optical output power more than 20%. Wafer or wafers from each production lot are tested.

3.7. FINAL DIE ACCEPTANCE CRITERIA

The flow chart below outlines the die-on-tape process and verification procedure, and the final wafer acceptance. Wafer qualification refers to the process of ensuring that each wafer or wafer lot meets the reliability standards in Section 2.6

Flow-Chart

4. DEVICE PHYSICAL LAYOUT

Refer to Vixar drawing 100680 for VCSEL chip specification

Parameter	Specification
Die size (x / y) final	0.175 mm X 0.215mm
Aperture Size	7 µm
Aperture Pitch	30 µm
Number of Apertures	3
Die thickness	100 µm

5. DATA REPORTING AND ARCHIVING

OSRAM requires that procedures are established to notify OSRAM in case of semiconductor product and process changes that impact the form, fit, function, or reliability of the VCSEL. These procedures are described in JEDEC Standard No. 46-D

In order to facilitate wafer and die processing using electronic wafer maps subsequent to wafer probing and AOI, as well as to facilitate product traceability for cost and quality management purposes, all measurements at all test points and conditions prescribed by this specification in Section 2.2.3 must be recorded for each unique die location and be preserved in an electronic data file at Vixar.

6. TERMS OF DELIVERY

Delivery of singulated VCSEL wafer will be on a 8inch Metal Film Frame Hoop ring. Part number of this product is Perfection product FF-108 or equivalent. The dicing tape is a Lintec D-175 UV tape, which will not be pre-exposed to UV radiation at the Foundry. The hoop ring will consist of a fully diced VCSEL wafer or section of wafer and will comprise both passing and failing VCSEL die. Each singulated wafer on tape will be accompanied by an electronic wafer pick map compliant with the KLA electronic mapping standards.

Singulated wafers on grip rings will be packaged in an ESD safe single wafer grip ring containers. Wafer containers will be vacuum sealed in ESD safe packaging. Both the exterior of the vacuum sealed packaging and wafer grip ring container will be labeled according to Section 5.1.1. The shelf life of the Lintec grip tape is 8 months when stored at 23°C ± 5°C in a dark location. Avoid storing the tape at high temperature (>28°C) or high humidity (>80% RH). We suggest not to leave the product mounted onto the tape after UV irradiation for more than 2 weeks. The shelf life of the hermetic ESD bag is 1 year. Vixar is not liable for malfunctioning product if the shelf life's have been exceeded.

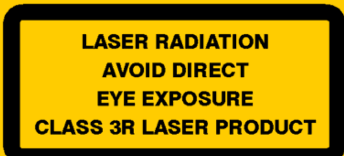
6.1.1. Barcode-Product-Label (BPL)

OSRAM Opto
Semiconductors
LX XXXX
BIN1: XX-XX-X-XXX-X
RoHS Compliant
(6P) BATCH NO: 1234567890
ML Temp ST
X XXX °C X
(1T) LOT NO: 1234567890
(9D) D/C: 1234
Pack: RXX
DEMY XXX
X_X123_1234.1234 X
(X) PROD NO: 123456789 (Q)QTY: 9999 (G) GROUP: XX-XX-X-X
EXAMPLE

OHA04563

Revision History

Revision	Date	Change Description
01	09/17/2019	Initial release
A	06/24/2021	Added Propel PN. Edited Section 3.2.1 Removed section 3.2.2 Corrected die size info & PN in section 4.
B	11/08/2021	Edited Ith Max spec and added a note.
C	06/13/2023	VF Operating voltage spec change upper limit from 2.25V to 2.05V in 3.2.1
2.0	December 11th - 2023	Update Ordering Code, Product Number and Barcode-Product-Label (BPL).



COMPLIES WITH IEC 60825-1, 2nd Edition 2007.
COMPLIES WITH 21 CFR 1040.10 AND 1040-10.11 EXCEPT FOR DEVIATIONS PURSUANT TO LASER NOTICE NO.50 DATED 27 MAY 2001.